CLAIMS

1. A multi flip chip module comprising:

a leadframe having a die pad with upper and lower surfaces and a plurality of outer leads surrounding the die pad;

an integrated circuit mounted on the upper surface of the die pad and having contact areas for receiving bond wires;

bond wires extending from the contact areas on the integrated circuit to the outer leads of the leadframe;

one or more power mosfet semiconductor devices flip chip mounted on the lower surface of the leadframe; and

a molded resin encapsulating the integrated circuit and leaving exposed at least one surface of the power mosfet semiconductor devices.

2. The multichip module of claim 1 wherein the mosfets have source bump contacts extending from the surfaces of the mosfets to the half etched die pad and one or more gate bump contacts for each mosfet extending to a corresponding outer lead.

3. The multichip module of claim 1 wherein the lead frame has leadless contacts comprising a of ball contacts extending from the outer leads for establishing an electrical connection to the contact areas of the integrated circuit via the bond wires and for providing surface mounts for connecting the semiconductor device to a surface of an electrical component board.

4. The multichip module of claim 1 wherein exposed surface(s) of the power mosfets are surface mountable on an electrical component board.

5. A multichip module having a lead frame with a central die pad and peripheral outer leads, an integrated circuit on one side of the die pad, wire bonds for connecting the integrated circuit to outer leads, one or more mosfets having their respective source and gates bump connected to the other side of the central die pad, said central die pad patterned to provide connections to the outer leads from the source and gate bump connections.

6. The multichip module of claim 5 wherein the integrated circuit is encapsulated in an insulating resin.

7. A method for manufacturing a multichip module comprising the steps of;

providing a lead frame with a central die pad having upper and lower surfaces and disposed between opposite lead rails having outer lead areas

etching the lower surface of the central die pad and the rails to provide raised lands for receiving source and gate contacts of one or more mosfets;

attaching an integrated circuit to the upper surface of the central die pad;

wire bonding contact areas of the integrated circuit to the outer lead areas on the leadframe rails;

encapsulating the integrated circuit in an electrically insulating resin;

bump attaching the source and gate of one or more mosfets to the raised lands on the lower side of the central die pad.

8. The method of claim 9 wherein the leadframe adheres to a tape and the tape is removed after the step of encapsulating.